COMPOSITE ETCHING STOP IN SEMICONDUCTOR PROCESS INTEGRATION

<This application is a CON. of 09/970,787 dated 10/5/01, PAT. 6753260>

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of metallization in the fabrication of integrated circuits, and more particularly, to a method of forming an improved etch stop layer for metallization in the manufacture of integrated circuits.

(2) Description of the Prior Art

In a common application for integrated circuit fabrication, a contact/via opening is etched through an insulating layer to an underlying conductive area to which electrical contact is to be made. A conducting layer material is deposited within the contact/via opening. The damascene and dual damascene processes have become a future trend in metallization. Trenches or vias and trenches are etched in an insulating layer. The trenches or vias and trenches are inlaid with metal to complete the contacts. In all of these processes, etch stop layers are required to accurately form the trenches and vias. A silicon carbide etching stop layer has a good copper diffusion barrier capability and a lower dielectric constant than silicon